At page 2, line 4, change "Documents [2] and [3]" to --U. Kleis, et al., *Doman Decomposition Methods for Circuit Simulation*, Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS, Edinburgh, UK (July, 1994), pp. 183-86, and U. Wever, et al., *Parallel Transient Analysis for Circuit Simulation*, Proceedings of the 29th Annual Hawaii International Conference on System Sciences (1946), pp. 442-47--.

At page 2, line 8, change "Document [4]" to --B. Riess, *Partitioning Very Large Circuits Using Analytical Placement Techniques*, Proceedings of the 31st ACM/IEEE Design Automation Conference (1994), pp. 646-51--.

At page 2, line 21, change "[5]" to --P. Johannes, *Partitioning of VLSI Circuits and Systems*, 33rd Design and Automation Conference, Las Vegas (June 3-7, 1996), pp. 83-87--.

At page 2, line 23, change "[6]" to --J. Cong, et al., *A Parallel Bottom-Up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Design*, 30th ACM/IEEE Design Automation Conference, June 14-18, 1993, pp. 755-760--.

At page 2, line 24, insert the following title:

--SUMMARY OF THE INVENTION--

At page 2, line 24, after inserting the above title, change "The method [sic] is thus based on the problem of specifying" to --The present invention provides--.

At page 2, line 27, delete the sentence "The problem is solved by the method accordin to patent claim 1." and insert the following paragraph:

--To that end, in an embodiment the invention provides a computer-supported method for partitioning an electrical circuit,

- whereby the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit,

- whereby edges of the graph have weighting values allocated to them with which a required calculating outlay for determining electrical descriptive quantities for elements of the electrical circuit that are represented by the respective edge is described,

- whereby a first sum value of the weighting values of the edges is calculated for edges coupled to one another and, in further iterations, the first sum value is respectively formed upon addition of at least one further edge until the respectively calculated, first sum value is greater than a prescribable, first threshold,

- whereby a partition of the electrical circuit is formed by the edges taken into consideration in the formation of the first sum value,

- whereby the following steps are implemented for at least a part of the remaining edges that do not lie in the partition and that are coupled to at least one edge of the partition:

- a second sum value is determined that derives from the sum of the first sum value and at least one weighting value of at least one remaining edge,

- when the second sum value is smaller than a prescribable second threshold, and

- when a plurality of edges that were taken into consideration in the formation of the second sum value that are coupled to edges that were not taken into consideration in the formation of the second sum value is smaller than a plurality of edges of the partition that are coupled to the remaining edges, then

- the remaining edge is allocated to the partition and the second sum value is allocated to the first sum value, and

- whereby the partition is formed by the edges taken into consideration in the formation of the second sum value.--

At page 3, line 12, change "document [4]" to --B. Riess in *Partitioning Very Large Circuits Using Analytical Placement Techniques*, Proceedings of the 31st ACM/IEEE Design Automation Conference (1994) pp. 646-651.--

At page 3, line 15, change "upon employment of" to --employing--.

At page 3, line 16, delete "inventively"; same line, after "determined" insert --in accordance with the invention--.

At page 4, lines 3-4, delete "Advantageous developments of the invention derive from the dependent claims." and insert the following:

--In an embodiment of the invention, at the beginning of the method, a grouping of elements of the electrical circuit is executed for which it is respectively found that these elements are allocated in common to a partition.

In an embodiment of the invention, at least one of the following rules is applied in the grouping of the elements of the electrical circuit:

- elements of a controlled source, at least one controlling element, and the controlled source are allocated in common to a partition,

- connecting loops in the electrical circuit that only contain at least one voltage source and at least one counter-inductance are allocated in common to a partition,

- no shorts dare arise due to the partitioning.

In an embodiment of the invention, a plurality of edges of the graph have a common weighting value allocated to them.

In an embodiment of the invention, the graph of the partition is mapped onto the electrical circuit, whereby the partition comprises the elements of the electrical circuit corresponding to the implemented partitioning.

In an embodiment of the invention, the method comprises the steps of iterating the method a plurality of times thereby forming a plurality of partitions, and determining electrical descriptive quantities for the elements of the electrical circuit for each partition, at least a part of the partitions being processed in parallel on a plurality of computers and/or processors.

In an embodiment of the invention, the parallel processing of the partitions is centrally controlled.

In an embodiment of the invention, at least a part of the partitions is centrally controlled in such a way that all terminals of the respective partition are coupled only to a central control unit, and a communication of data ensues only between the central control unit and at least the part of the partitions.

In an embodiment of the invention, a voltage source is additionally allocated at least to a part of the terminals of the respective partition, the value of said additional voltage predetermined by the central control unit during the determination of the electrical descriptive quantities.

In an embodiment of the invention, a resistor is additionally allocated at least to a part of the terminals of the partition.

At page 4, lines 22-24, delete "The Figures show an exemplary embodiment of the method that is explained in greater detail below. Shown are:" and insert the following paragraph:

--These and other features and aspects of the invention will become clear in the following detailed description of a few typical exemplary embodiments with reference to the accompanying drawings.--

At page 4, line 24, insert the title:

--BRIEF DESCRIPTION OF THE DRAWINGS--.

At page 4, line 25, after "Fig. 1" insert --is--.

At page 4, line 26, after "Fig. 2" insert --is--.

At page 4, line 27, insert the following heading:

--DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS--

At page 4, line 28, change "Electrical" to --In accordance with the invention, electrical--.

At page 5, line 10, change "the document [1]" to --L. Hoefer, et al. in *SPICE Analyseprogramm for electronische Schaltungen*, Springer, Berlin (1985), pp. 7-22.--

At page 5, line 14, change "In" to --With reference now to the figures, in--; same line, change "on" to --onto--.

At page 6, line 19, change "is basically uncritical" to --basically is not critical--.

At page 6, line 21, change "A n" to --An--.

At page 7, line 23, after "steps" insert --designated 108--.

At page 7, line 24, after "implemented" delete "108".

At page 7, line 29, after "formed" insert --at--.

At page 8, line 3, after "Si" insert --at--.

At page 8, line 11, after "added" insert --at--.

At page 8, line 18, after "coupled" insert --at--.

At page 8, line 22, change "described later [sic]" to --(described later)".

At page 8, line 26, after "added" insert --at--.

At page 8, line 28, after "added" insert --at--.

At page 9, line 7, after "employed" insert --at--.

At page 9, line 14, after "back-imaging" insert --at--.

At page 10, line 26, insert the following paragraph: